

1 1. A method comprising:
2 forming a phase change memory pore including a
3 breakdown layer and increasing the likelihood that the
4 breakdown will occur in one region rather than another
5 region of the layer.

1 2. The method of claim 1 including forming a phase
2 change memory pore by:
3 forming an electrode over a substrate;
4 forming a dielectric layer with an aperture; and
5 forming a breakdown layer over said electrode in
6 said aperture.

1 3. The method of claim 2 including forming a phase
2 change material over said layer and coupling said phase
3 change material between an upper conductive line and a
4 lower conductive line.

1 4. The method of claim 3 including coupling a lower
2 conductive line to said electrode through a selector
3 device.

1 5. The method of claim 1 including ion implanting a
2 portion of said layer to change the likelihood of breakdown
3 in that implanted portion relative to an unimplanted
4 portion of said layer.

1 6. The method of claim 5 including implanting at an
2 angle.

1 7. The method of claim 6 including forming a pore
2 defined in an insulator and implanting at an angle such
3 that said insulator acts as a mask to said ion
4 implantation.

1 8. The method of claim 1 including forming a
2 relatively centrally located within said pore that is more
3 likely to breakdown.

1 9. The method of claim 1 including forming a
2 relatively peripherally located region in said pore that is
3 more likely to breakdown.

1 10. The method of claim 1 including damaging one
2 region of said layer to change the likelihood that a
3 breakdown will occur in that region relative to another
4 region.

1 11. A memory comprising:
2 a breakdown layer between a pair of electrodes,
3 said breakdown layer being ion implanted to increase the
4 likelihood that breakdown will occur in one region rather
5 than another region of said layer.

1 12. The memory of claim 11 wherein said memory is a
2 phase change memory including a phase change material
3 between said electrodes.

1 13. The memory of claim 12 wherein said phase change
2 material is a chalcogenide.

1 14. The memory of claim 13 including a substrate and
2 a dielectric layer over said substrate with an aperture
3 formed therein, an electrode being positioned at the bottom
4 of said aperture and said breakdown layer being positioned
5 over said electrode in said aperture.

1 15. The memory of claim 14 wherein said phase change
2 material is over said breakdown layer.

1 16. The memory of claim 15 including an upper
2 conductive line over said phase change material and a lower
3 conductive line under said electrode.

1 17. The memory of claim 11 wherein said breakdown
2 layer is formed of an insulator.

1 18. The memory of claim 17 wherein said insulator
2 includes nitride.

1 19. The memory of claim 11 wherein a central portion
2 of said layer is ion implanted and a peripheral region of
3 said breakdown layer is not ion implanted.

1 20. A system comprising:
2 a processor-based device;
3 a wireless interface coupled to said processor-
4 based device; and
5 a semiconductor memory coupled to said device,
6 said memory including a pair of electrodes, a breakdown
7 layer between said pair of electrodes, said breakdown layer
8 being ion implanted to increase the likelihood that
9 breakdown will occur in one region rather than another
10 region of said layer.

1 21. The system of claim 20 wherein said memory is a
2 phase change memory including a phase change material
3 between said electrodes.

1 22. The system of claim 21 wherein said phase change
2 material is a chalcogenide.

1 23. A method comprising:
2 forming a breakdown layer between a pair of
3 electrodes and increasing the likelihood that breakdown

4 will occur in one region rather than another region of said
5 layer.

1 24. The method of claim 23 including forming a phase
2 change material between said electrodes.

1 25. The method of claim 23 including ion implanting
2 said breakdown layer.

1 26. A memory comprising:
2 a breakdown layer between a pair of electrodes,
3 said breakdown layer having a central region and a
4 peripheral region between said electrodes, such that
5 breakdown is more likely to occur in one of said regions
6 than the other of said regions.

1 27. The memory of claim 26 including a phase change
2 material between said electrodes.

1 28. The memory of claim 27 wherein said breakdown
2 layer is ion implanted.

1 29. The method of claim 28 including a dielectric
2 over a substrate, said dielectric having an aperture and
3 said breakdown layer being formed in said aperture.

1 30. The memory of claim 29 including an electrode at
2 the bottom of said aperture and another electrode over said
3 aperture, said phase change material being between said
4 electrodes.